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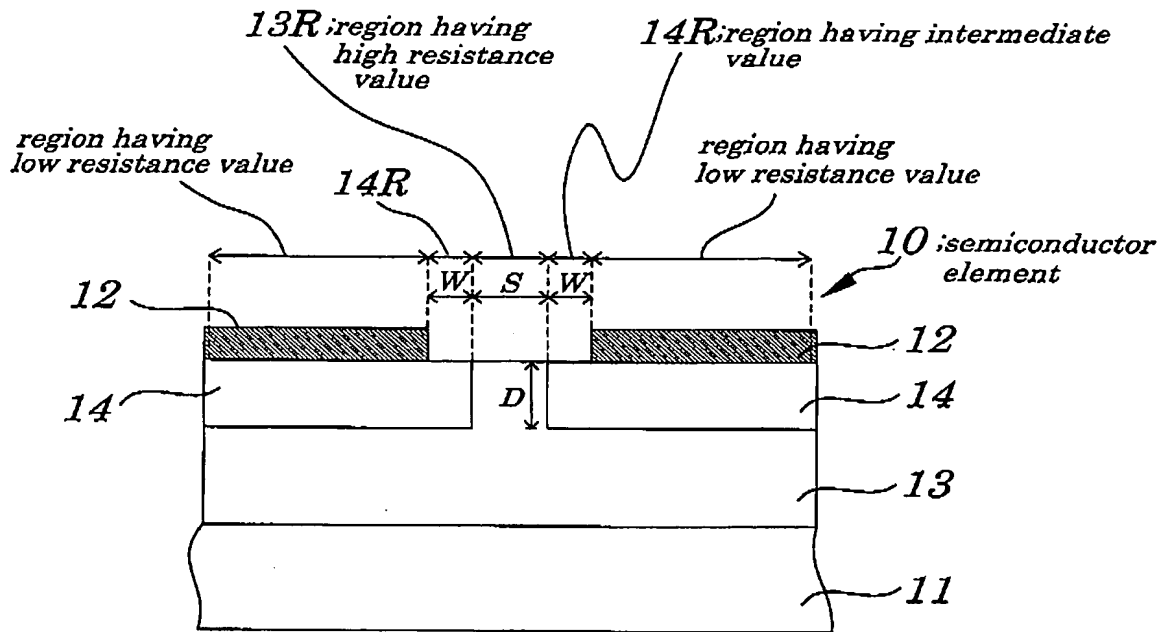
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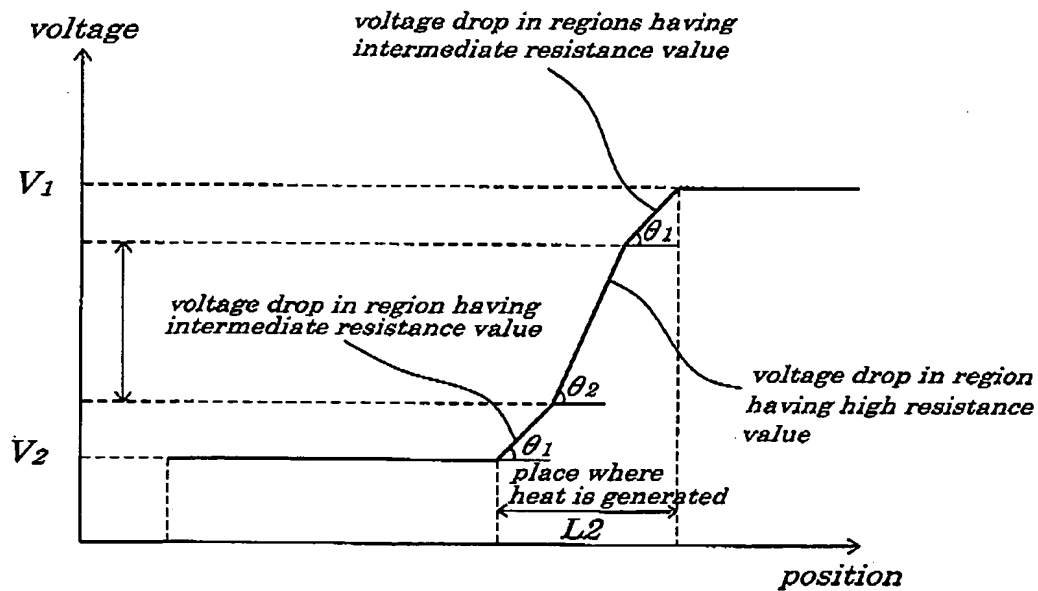
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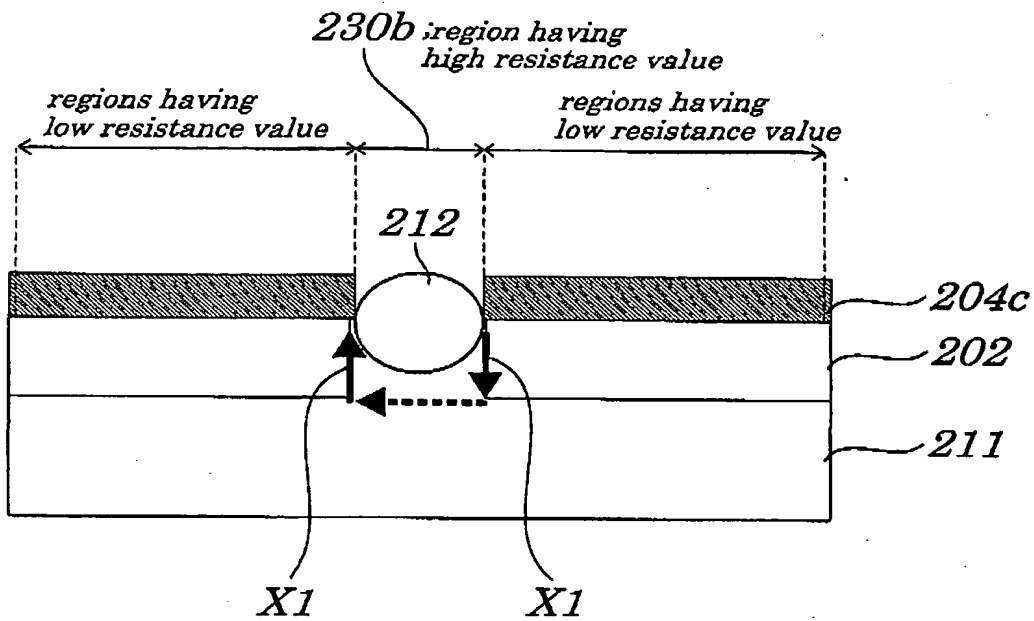
**FIG. 1**



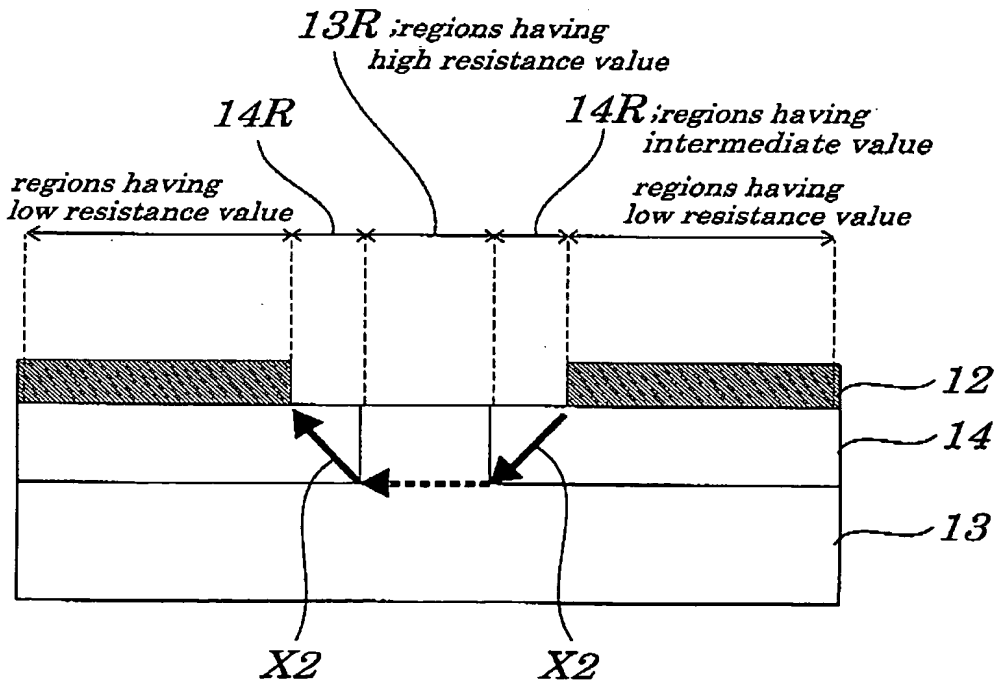
**FIG. 2**



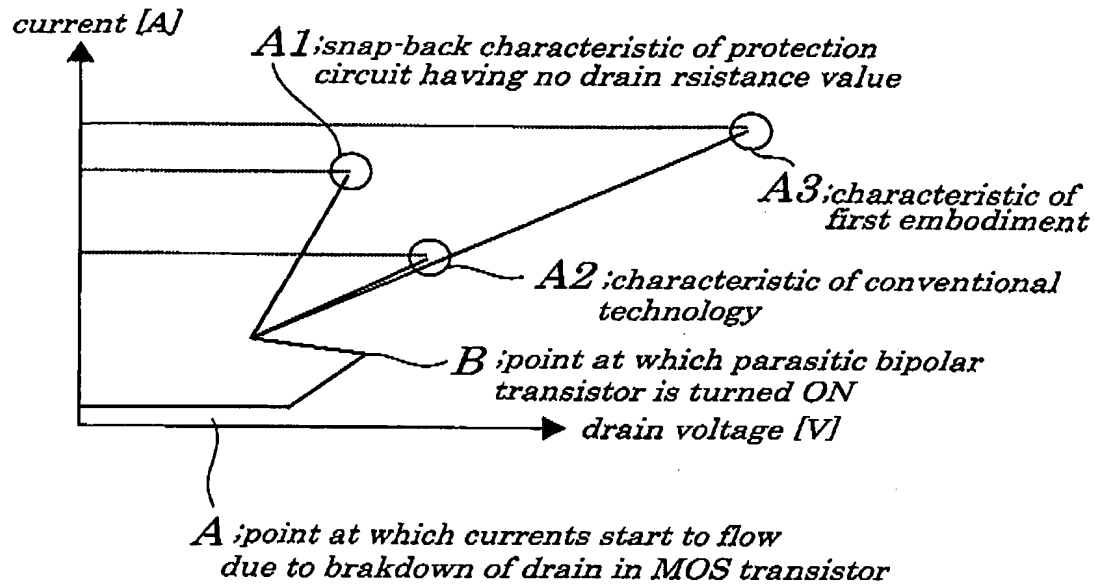
**FIG. 3A (PRIOR ART)**



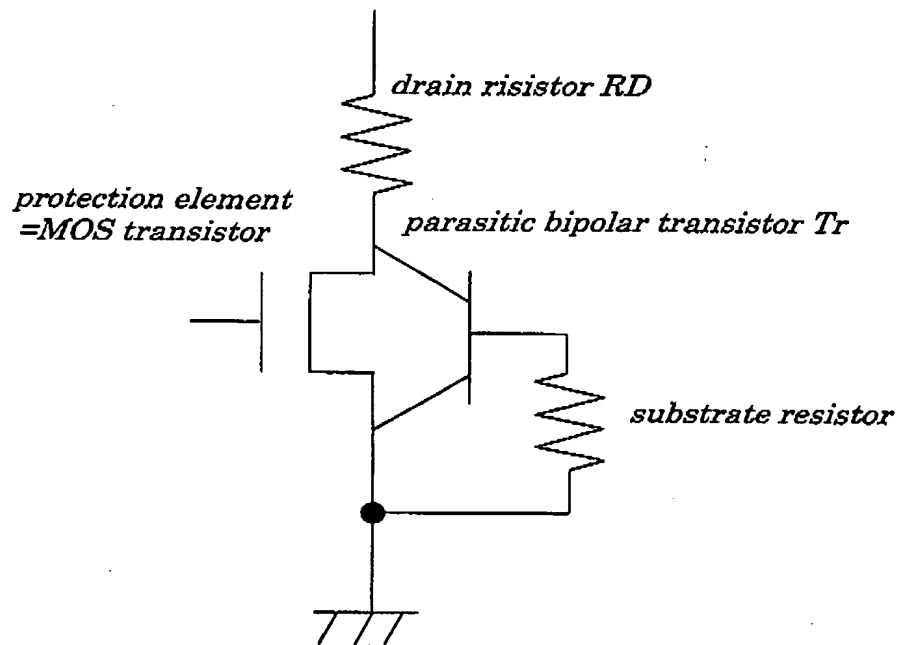
**FIG. 3B**



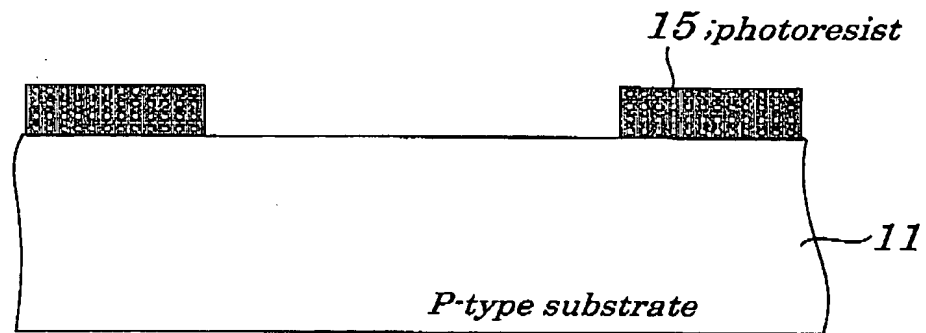
**FIG. 4A**



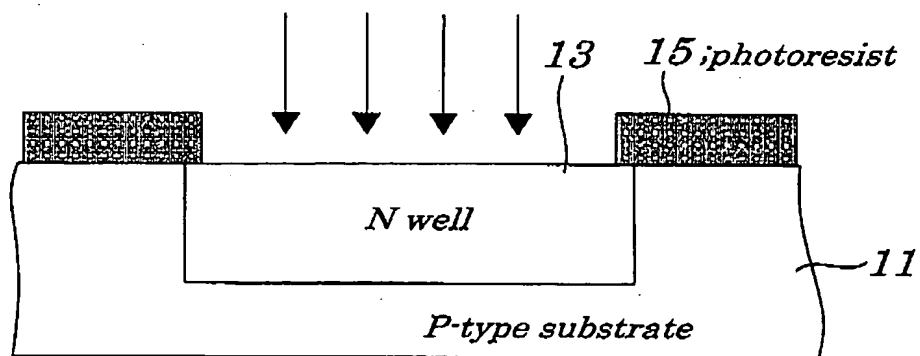
**FIG. 4B**



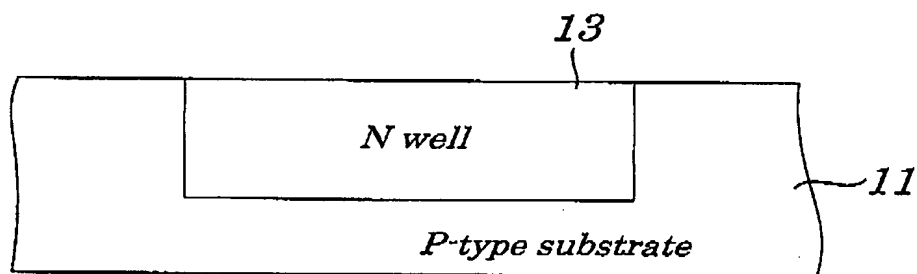
**FIG.5**



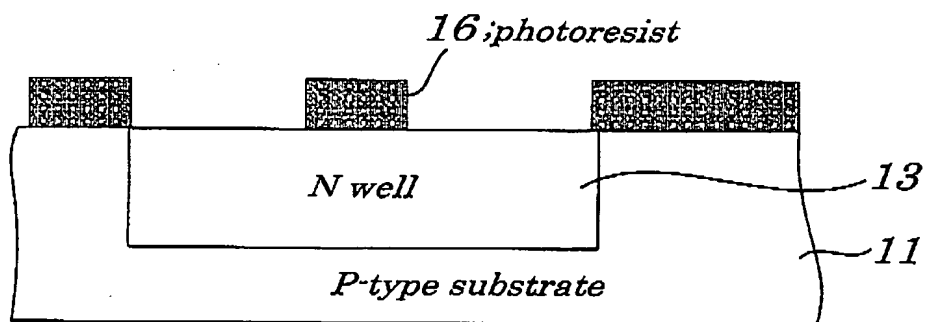
**FIG.6**



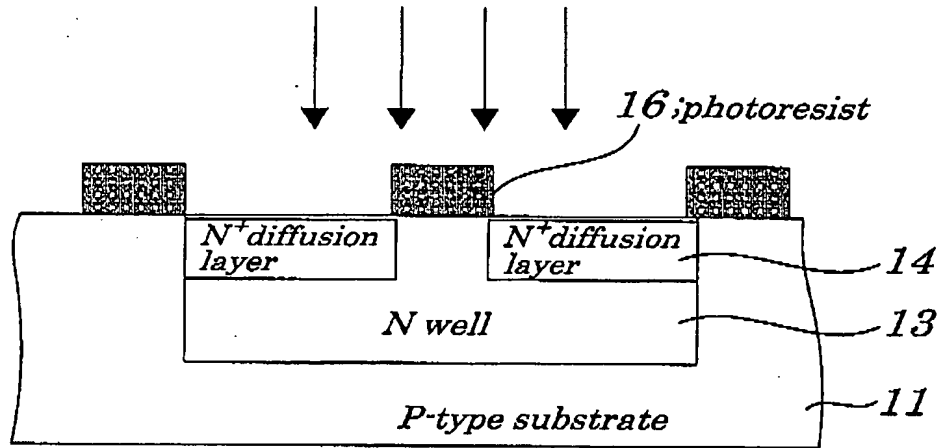
**FIG. 7**



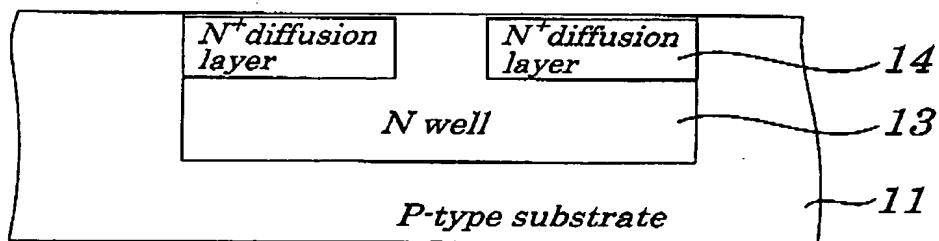
**FIG. 8**



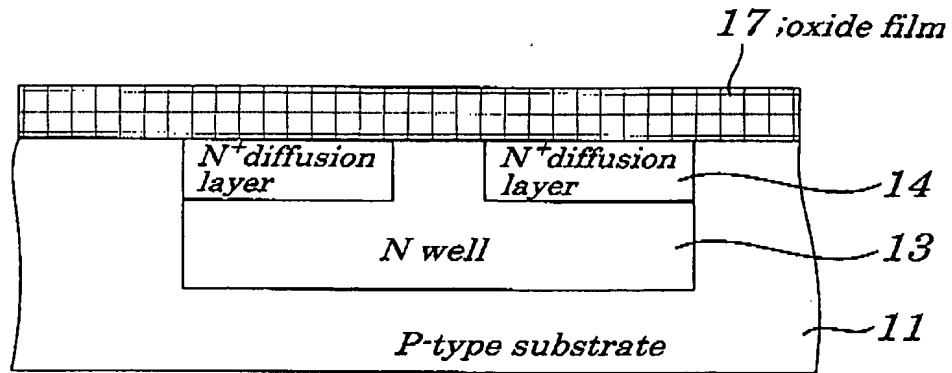
**FIG. 9**



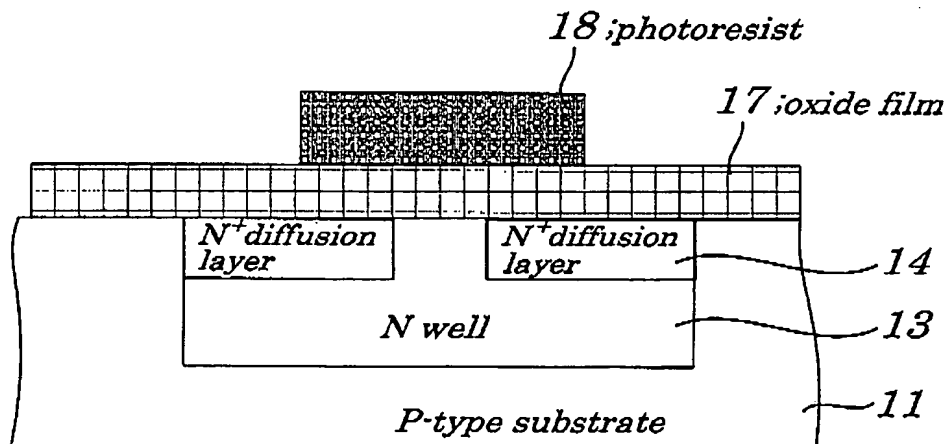
**FIG. 10**



**FIG.11**

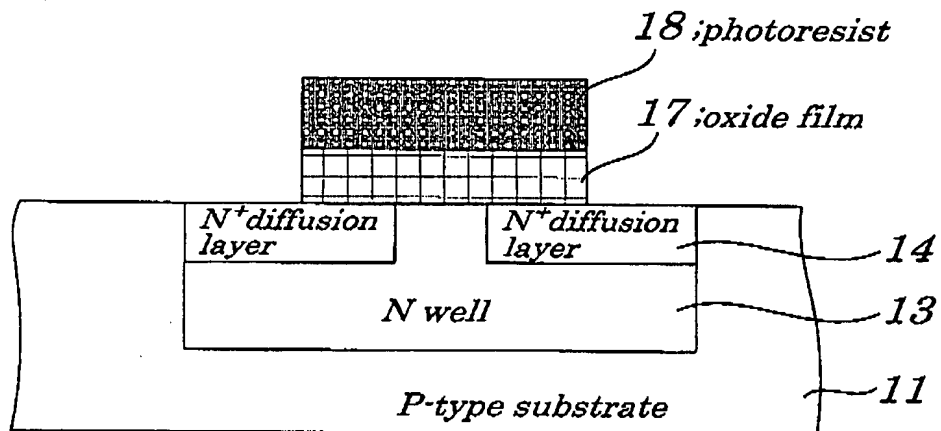


**FIG.12**

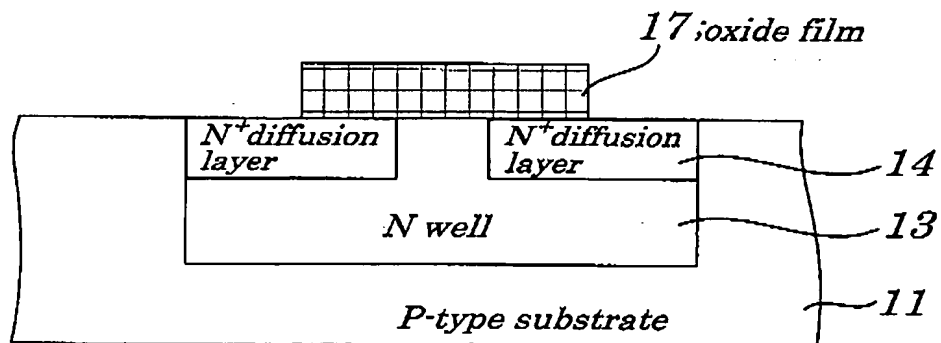




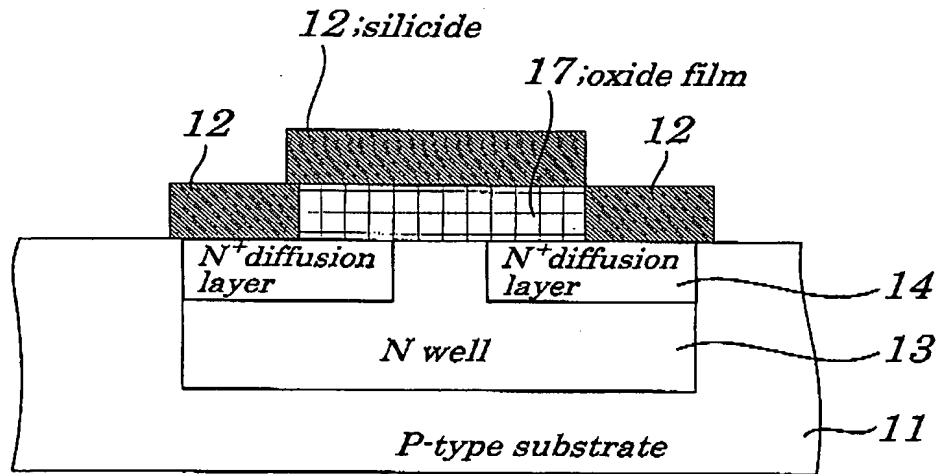
**FIG.13**



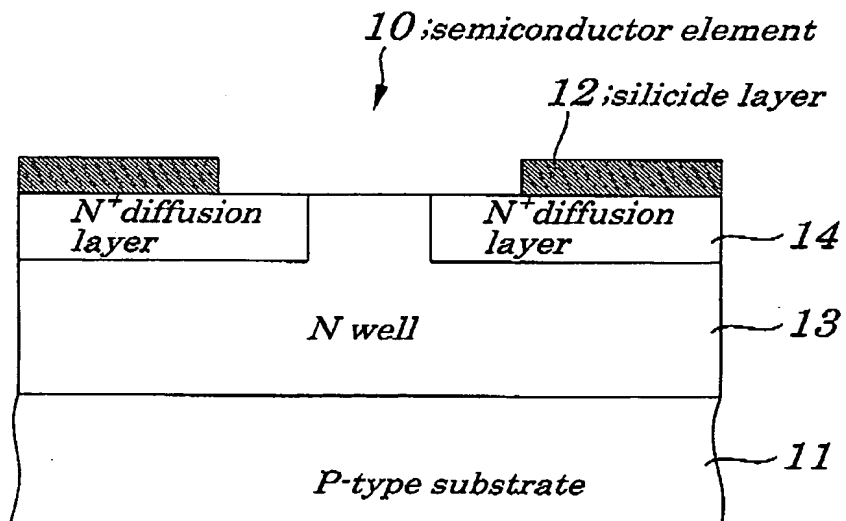
**FIG.14**



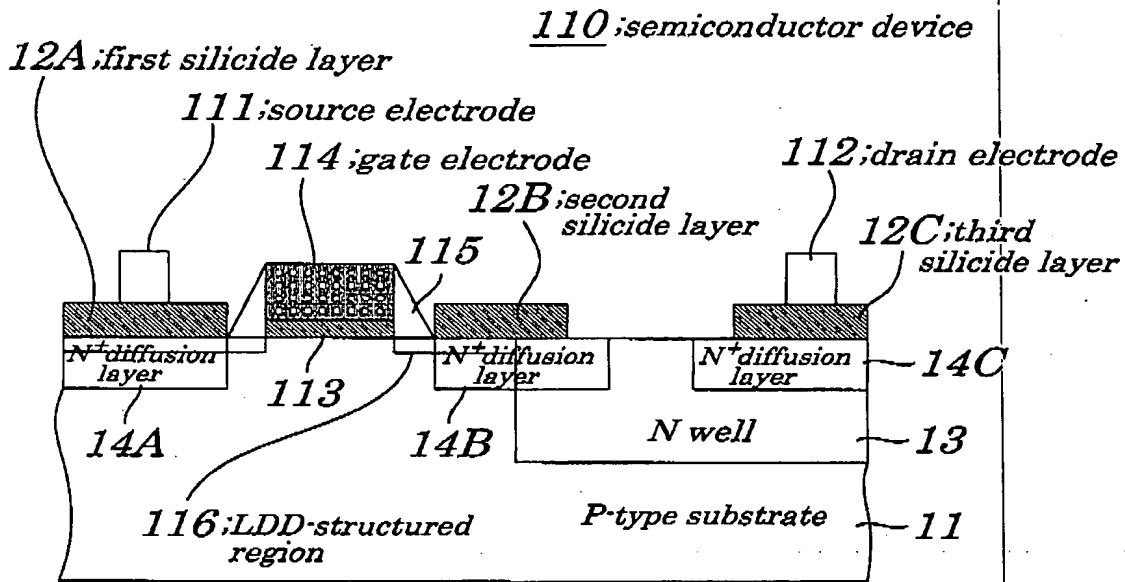
**FIG.15**



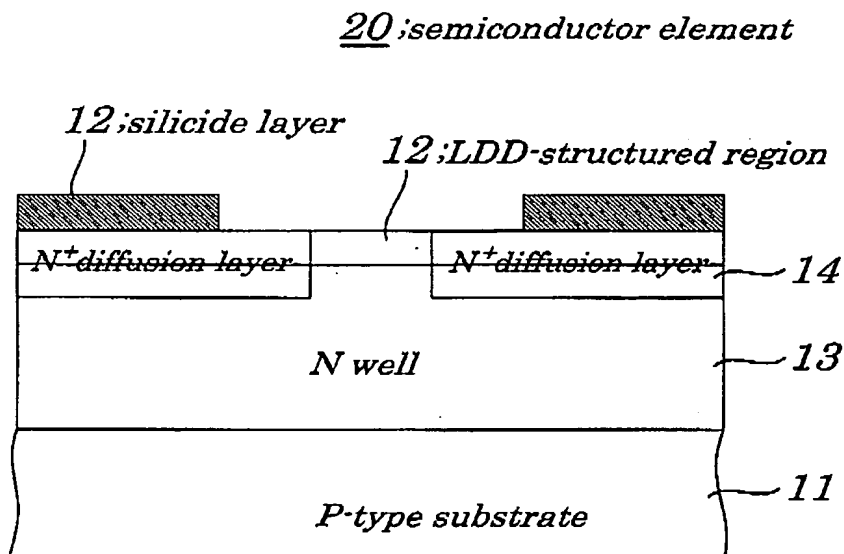
**FIG.16**



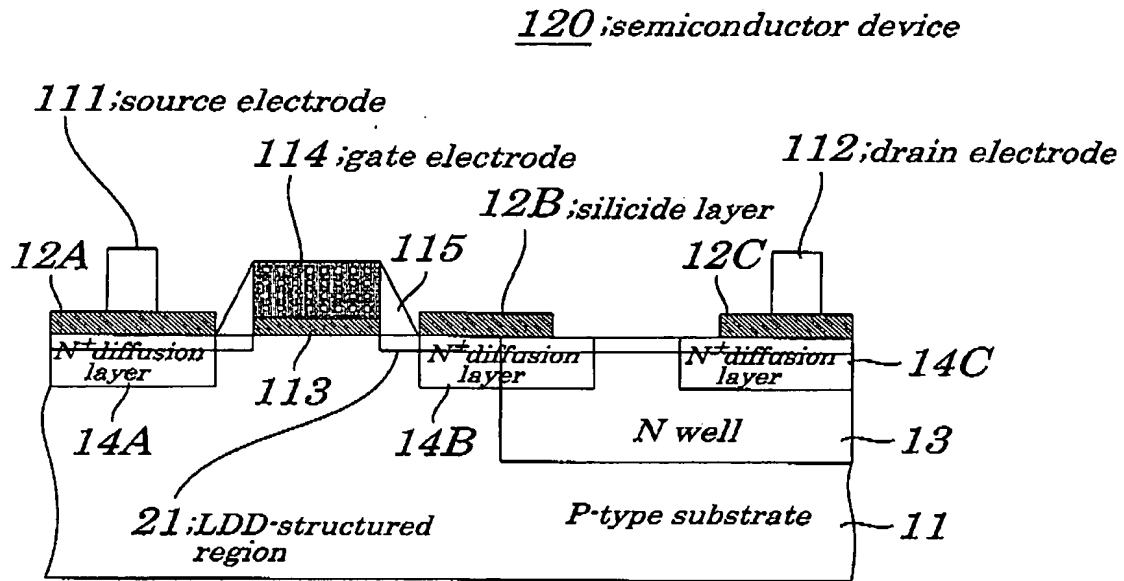
**FIG.17**



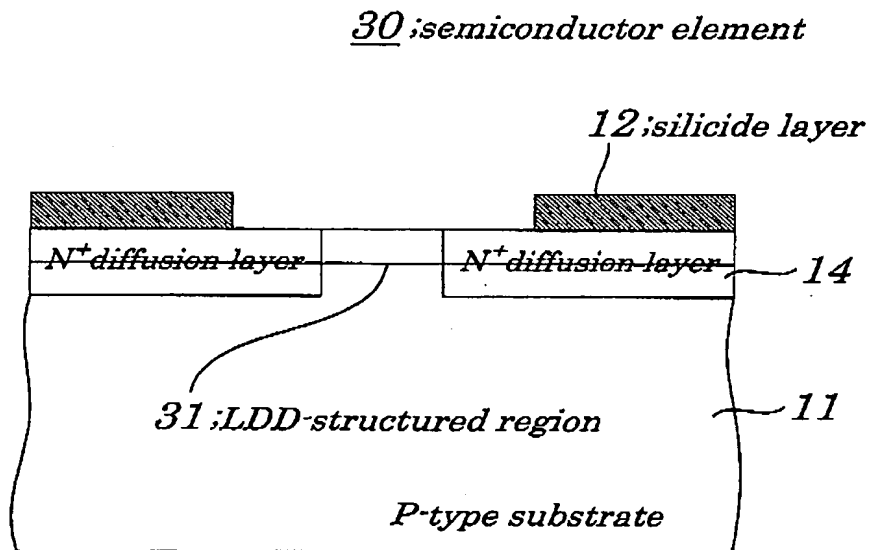
**FIG.18**



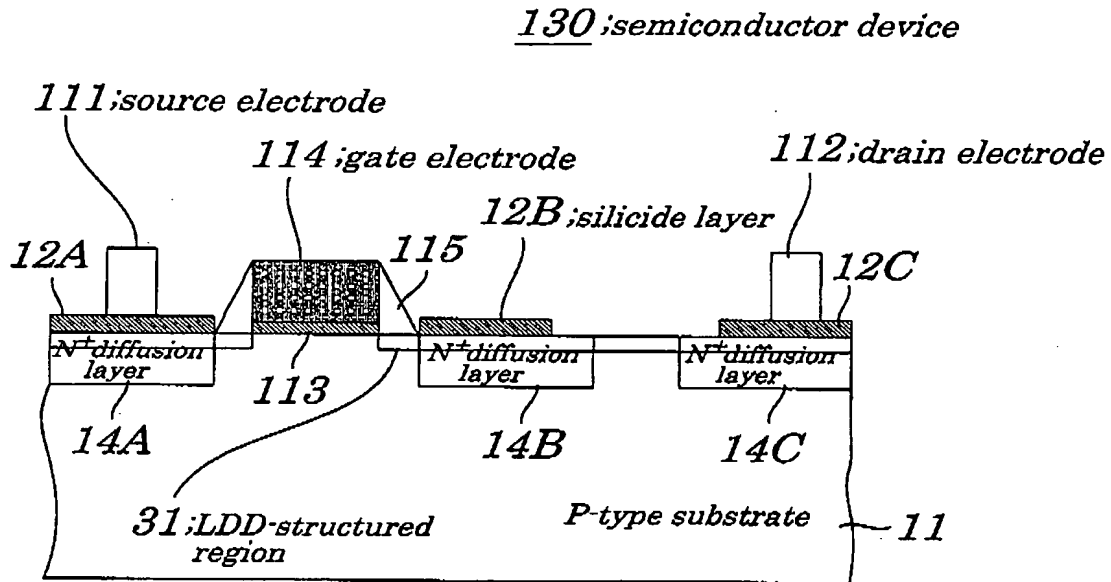
**FIG.19**



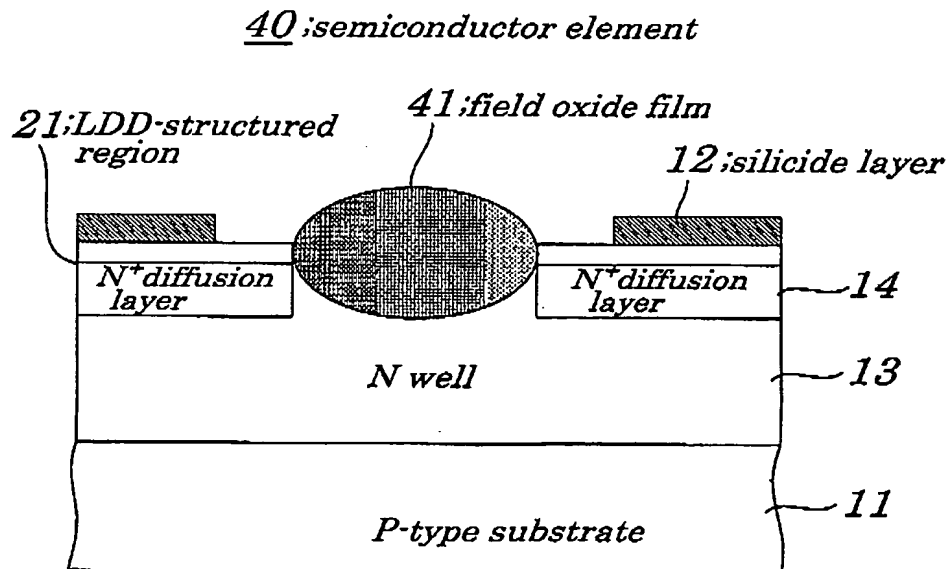
**FIG.20**



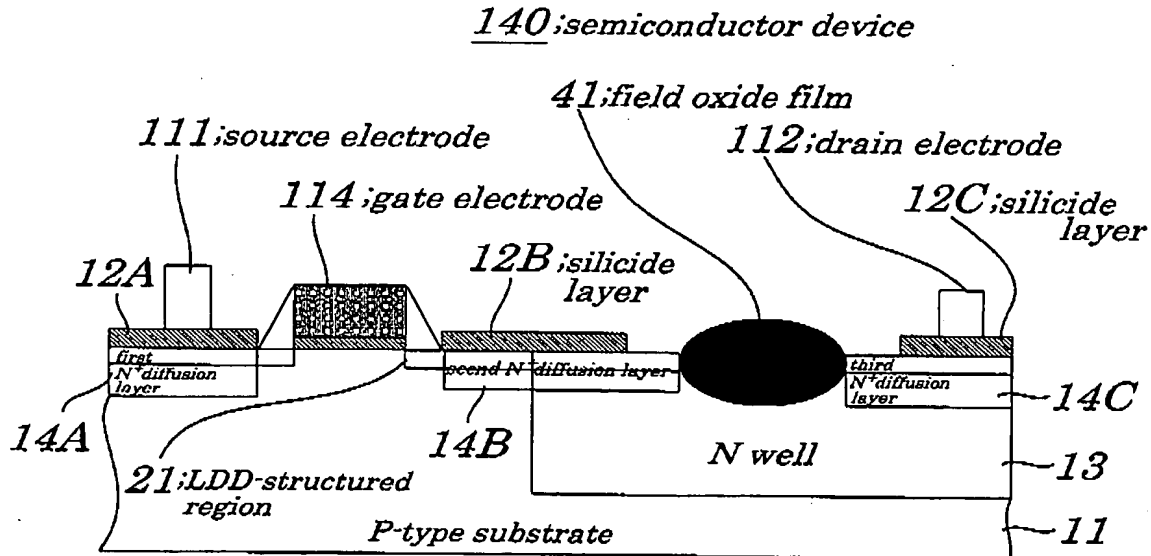
**FIG.21**



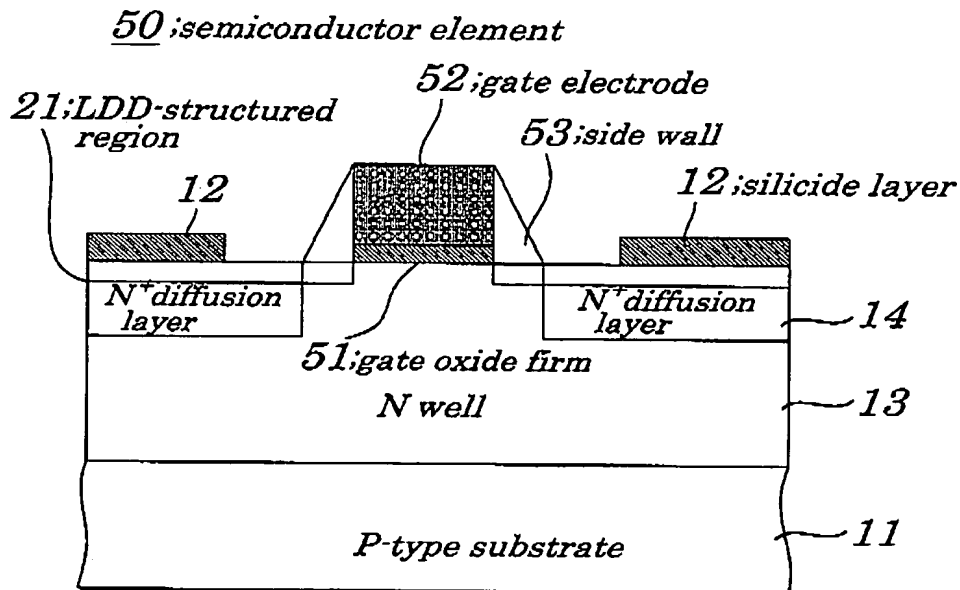
**FIG.22**



**FIG.23**

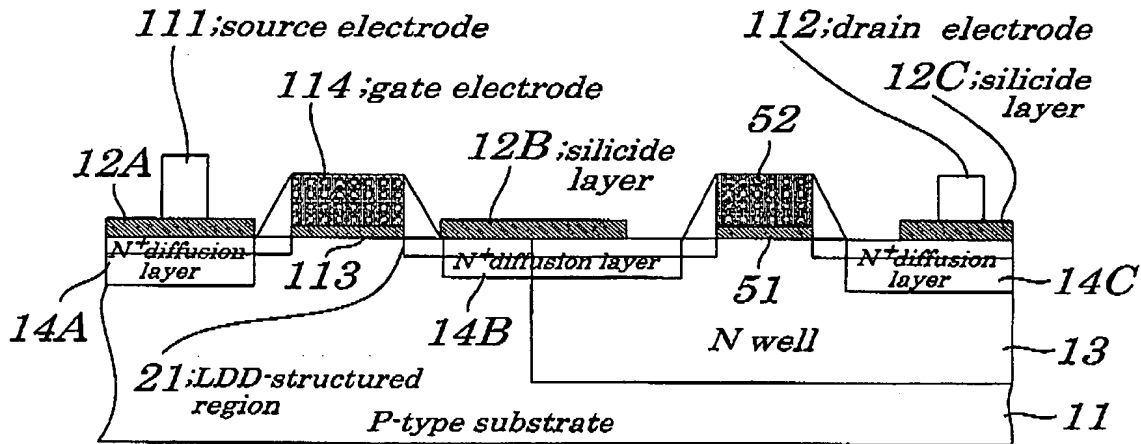


**FIG.24**



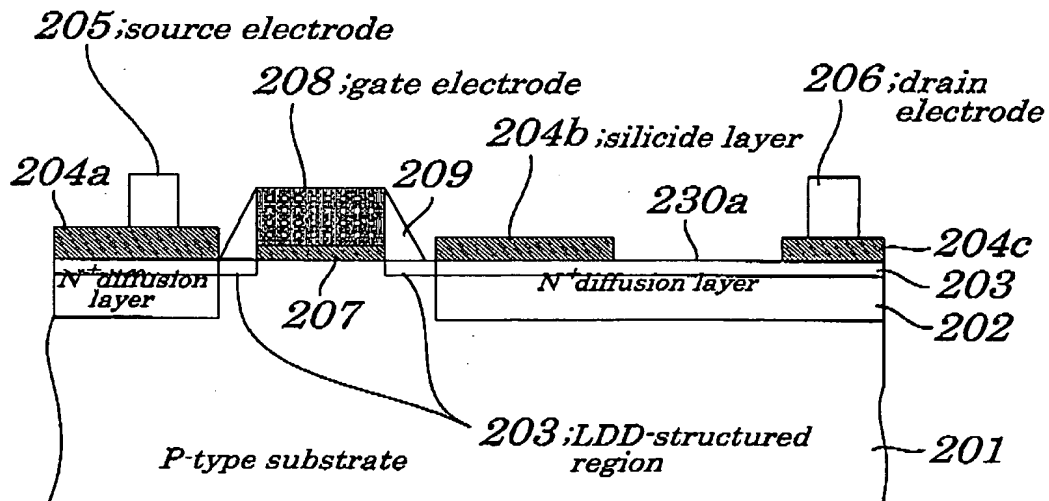
**FIG.25**

150;semiconductor device



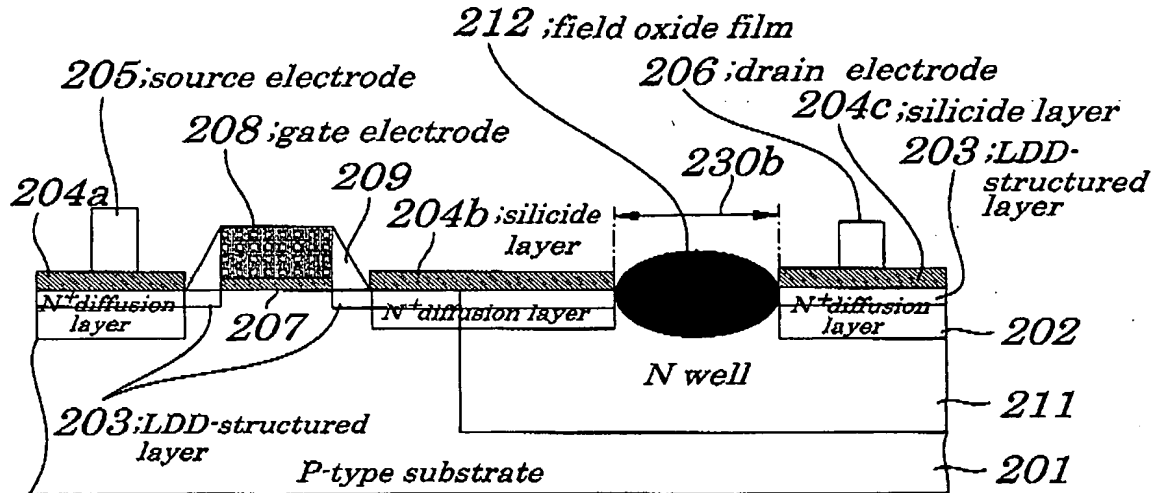
**FIG.26 (PRIOR ART)**

200;semiconductor device



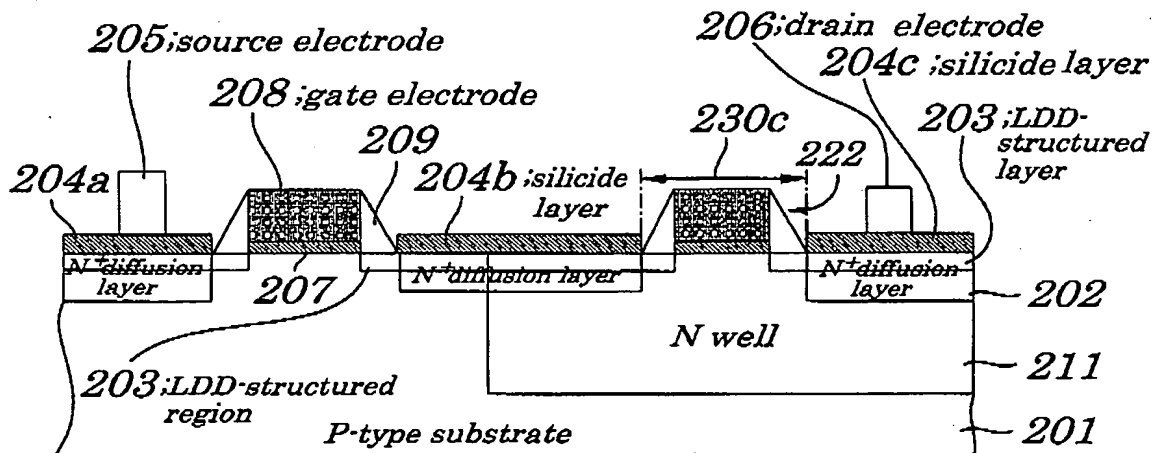
**FIG.27 (PRIOR ART)**

210;semiconductor device



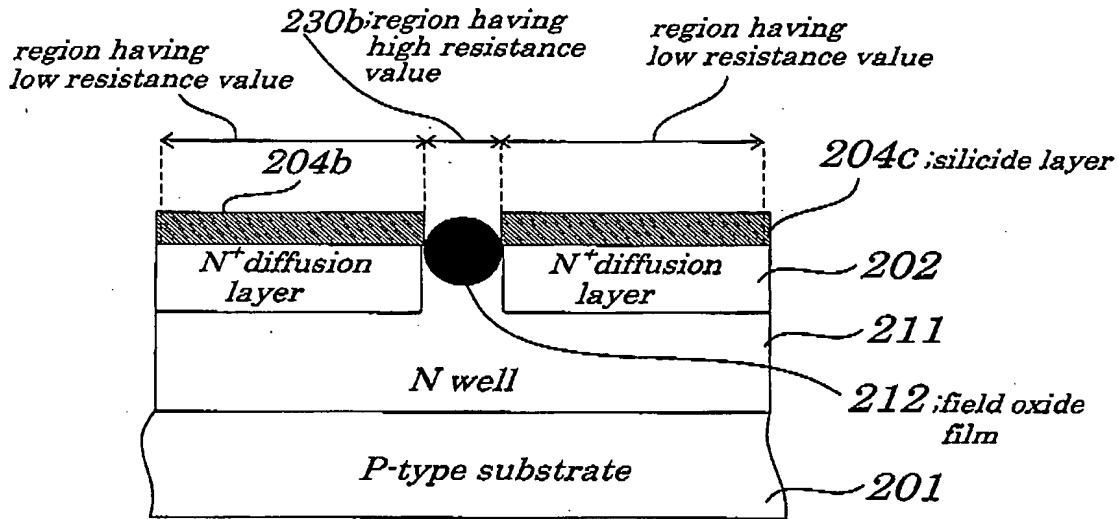
**FIG.28 (PRIOR ART)**

220;semiconductor device





**FIG. 29A (PRIOR ART)**



**FIG. 29B (PRIOR ART)**

